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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,874	01/20/2004	Kent Kuohua Chang	9945-US-PA-1	1873

31561 7590 11/15/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
TOLEDO, FERNANDO L	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/707,874	CHANG, KENT KUOHUA	
	Examiner	Art Unit	
	Fernando L. Toledo	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 8 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U. S. Patent 6,420,237 B1) in view of Wong (U. S. Patent 6,747,896 B2).

In re claim 8, Chang, in the U. S. Patent 6,420,237; figures 1 – 9 and related text discloses, providing a substrate 82; forming a tunneling oxide layer 84 on the substrate; forming a conductive layer 86 on the tunneling oxide layer; forming an isolation layer 87 in the conductive layer to partition the conductive layer into more than two conductive blocks arranged in an array with several rows extending from a region predetermined for forming one bit line to another region predetermined for forming another bit line and several columns, where each row includes n (n is a positive integer) conductive blocks (Figures 7 and 8); forming a gate dielectric layer 90 on the conductive layer; patterning the gate dielectric layer and the conductive layer to form a floating gate (Figure 6); forming the bit lines 96 in the substrate at two sides of the floating gate; forming a control gate 98 on the floating gate.

Chang does not show performing a step of threshold voltage adjustment to result in different threshold voltages of the channel regions under the conductive blocks of different rows.

However, Wong, in the U. S. Patent 6,747,896 B2; figures 1 – 10E discloses performing a step of threshold voltage adjustment to result in different threshold voltages of the channel regions under the conductive blocks of different rows (Figures 4A – 4D) to increase storage capacity (Column 1, Lines 6 and 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform a step of threshold voltage adjustment to result in different threshold voltages of the channel regions under the conductive blocks of different rows in the invention of Chang, since, as disclose by Wong, it increases the storage capacity.

3. In re claim 9, Chang discloses wherein the material of the conductive layer includes germanium polycide (Column 3, Lines 7 – 13).

4. In re claim 10, Chang discloses forming a patterned photoresist layer 88 on the conductive layer to expose a part of the conductive layer predetermined for forming the isolation region (Figure 5); performing an ion implantation step to implant dopant into the exposed conductive layer (Figure 5); and performing an annealing process to react the dopant with silicon of the conductive layer to form the isolation region (Column 3, Lines 32 – 34).

5. In re claim 11, Chang discloses wherein the dopant includes oxygen ions (Column 4, Line 29).

6. In re claim 12, Chang discloses wherein ion implantation step is performed with a dosage of dopant of about $1x10^{18}$ atoms/cm^2 to about $2x10^{18}$ atoms/cm^2 (Column 4, Lines 28 – 32).

7. In re claim 13, Chang discloses wherein the ion implantation step is performed with an implantation energy about 20 KeV to about 80 KeV (Column 4, Lines 28 – 32).

8. In re claim 14, Chang discloses wherein the dopant includes nitrogen ions (Column 4, Line 36).

9. In re claim 15, Chang discloses wherein the annealing process is performed at about 950°C to about 1150°C (Column 4, Line 33).

10. In re claim 16, Chang discloses further including a step of forming a field oxide layer 97 after a step of forming the bit lines and before the step of forming the control gate.

11. In re claim 17, Chang, in the U. S. Patent 6,420,237; figures 1 – 9 and related text discloses, providing a substrate 82; forming a tunneling oxide layer 84; forming a germanium polycide layer 86 on the tunneling oxide layer; forming a patterned photoresist layer 88 on the germanium polycide layer, the patterned photoresist layer exposing a part of the germanium polycide layer predetermined for forming an isolation region 87; performing an ion implantation step to implant dopant into exposed germanium polycide layer (Figure 5); performing an annealing process to react the dopant with silicon of the germanium polycide layer to form an isolation region that partitions the germanium polycide layer into more than two conductive blocks arranged in an array with several rows extending from a region predetermined for forming one bit line to another region predetermined for forming another bit line and several columns, where each row includes n (n is a positive integer) conductive blocks (Figures 7 and 8); forming a gate dielectric layer 90 on the germanium polycide layer; patterning the gate dielectric layer and the conductive layer to form a floating gate (Figure 6); forming the bit lines 96 in the substrate at two sides of the floating gate; forming a control gate 98 on the floating gate.

Chang does not show performing a step of threshold voltage adjustment to result in different threshold voltages of the channel regions under the conductive blocks of different rows.

However, Wong, discloses performing a step of threshold voltage adjustment to result in different threshold voltages of the channel regions under the conductive blocks of different rows (Figures 4A – 4D) to increase storage capacity (Column 1, Lines 6 and 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform a step of threshold voltage adjustment to result in different threshold voltages of the channel regions under the conductive blocks of different rows in the invention of Chang, since, as disclose by Wong, it increases the storage capacity.

12. In re claim 18, Chang discloses wherein the step of ion implantation further includes implanting oxygen ions into the exposed germanium polycide layer (Column 4, Line 29).

13. In re claim 19, Chang discloses wherein the step of ion implantation further includes implanting nitrogen ions into the exposed germanium polycide layer (Column 4, Line 36).

14. In re claim 20, Chang discloses further including forming a field oxide 97 and a spacer 99 on a sidewall of the floating gate after the step of forming the bit lines and before the step of forming the control gate (Figure 7).

Response to Arguments

15. Applicant's arguments filed 2 September 2005 have been fully considered but they are not persuasive for the following reasons.

16. Applicant contests that Chang does not show more than two conductive blocks.

Examiner respectfully submits that Figure 7 of Chang shows at least 4 conductive blocks.

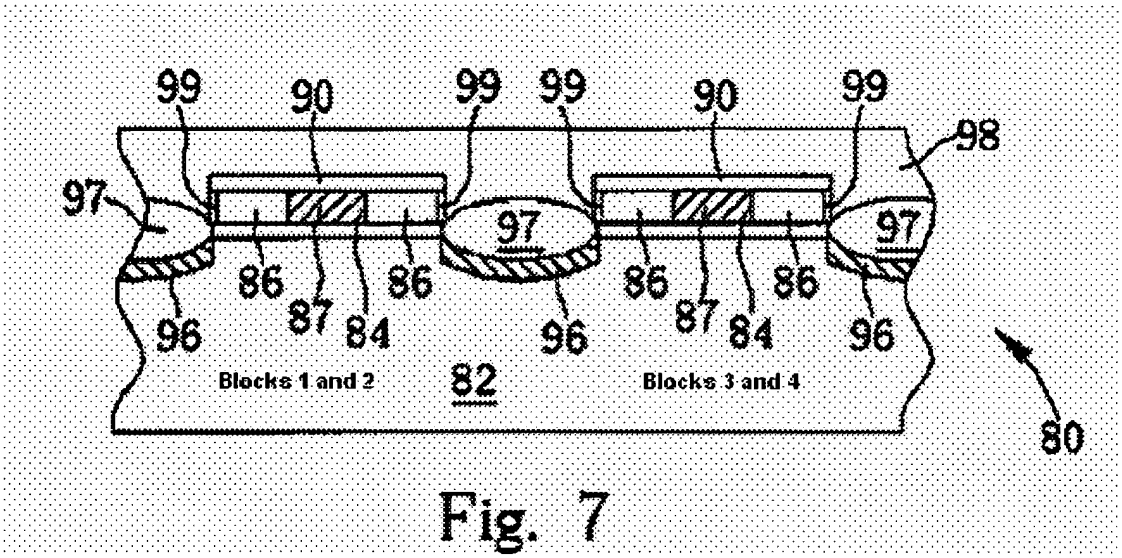

Fig. 7

Figure 7 has been modified to underscore that it shows the at least 4 conductive blocks.

Conclusion

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando L. Toledo whose telephone number is 571-272-1867. The examiner can normally be reached on Mon-Thu 7am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

George Fourson
Primary Examiner
Art Unit 2823

FToledo
2 November 2005